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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,576	DU ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9,18,23 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-9, 18, 23, and 26-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites "the removing...includes retaining at least one semiconductor layer...in the trench region" (ln 2-4). In light of the specification, it seems said semiconductor layer must be the window layer: additional layers are mentioned at pg 4 ln 23-24 but no support is provided for them being in the trench region, actually the implication is that they are part of the active region at pg 4 ln 25; the window layer is a semiconductor layer according to pg 5 ln 13, and is the only semiconductor layer with support for remaining in the trench region after the mesa etch (pg 5 ln 18-19), as shown in Fig 1. In other words, claim 7 describes forming a window layer prior to removing the substrate. Claim 7 depends from claim 2, which requires forming a window layer subsequent to removing the substrate (ln 10-11). Therefore, the above-recited limitation of claim 7 is impossible and it cannot be determined what the intended order of steps is. Claims 8 & 9 depend from 7 and inherent this indefiniteness

In view of the present amendments and remarks, it seems the independent (and thus all) claims are intended to require a window layer formed after substrate removal.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2, 4-7, 9, 18, 23, and 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Camras (US 6,784,463).

Re claim 2, Camras discloses a method of manufacturing a light emitting diode (col 3 ln 55-60, col 4 ln 9-12), the method comprising (e.g., Figs 4 & 6, col 11 ln 21-24):

depositing a plurality of semiconductor layers (112, 114, 116) on a deposition substrate (140, col 11 ln 25);

removing at least some of the deposited semiconductor layers from a selected trench region of the deposition substrate to define a light-emissive mesa (Fig 6D);

forming an electrode (118, col 11 ln 38) on the mesa (110 in Fig 5D);

flip-chip bonding (Fig 4, col 9 ln 30-32) the mesa to a first electrical bonding pad (134) of a thermally conductive (to any extent, as per MPEP § 2111) support (130);

removing the deposition substrate (col 11 ln 27); and

subsequent to the removing of the deposition substrate, depositing (col 11 ln 29) a light-transmissive, electrically conductive (transparent semiconductor: col 4 ln 64-65) window layer (117) on a surface of the mesa opposite the electrode, the window layer

extending laterally to electrically contact a second electrical bonding pad (138) of the thermally conductive support to define an electrical path between the mesa and the second electrical bonding pad (col 8 ln 12-23).

Re claim 4, Camras discloses depositing said semiconductor layers by a deposition technique selected from the group consisting of metalorganic chemical vapor deposition and molecular beam epitaxy (col 10 ln 27-34, col 11 ln 23-26), and depositing at least one window layer by liquid phase epitaxy (col 10 ln 60-62).

Re claim 5, Camras discloses non-epitaxially depositing (encompassed by "conventional deposition techniques", col 10 ln 60-62) at least one window layer.

Re claim 6, Camras discloses the removing of the deposition substrate effects a physical separation of the mesa wherein the mesa defines a separated light emitting diode device die flip-chip bonded to the thermally conductive support (e.g., Fig 4).

Re claim 7, Camras discloses retaining at least one semiconductor layer (114) that is substantially electrically conductive in the trench region, and

flip-chip bonding a second electrical bonding pad (138) to the retained semiconductor layer in the trench region (by way of 136 and 120), wherein the retained semiconductor layer defines an electrical path between the mesa (110) and the second bonding pad.

Re claim 9, Camras discloses the deposition substrate (140) is a GaAs substrate (col 10 ln 39-40), the plurality of semiconductor layers (112, 114, 116) include group III-phosphide layers (col 4 ln 32-33), and the retained semiconductor layer (114) includes a layer that contains aluminum (col 1 ln 29-31).

Re claim 18, Camras discloses a method of manufacturing a flip-chip (col 9 ln 30-32) light emitting diode (col 3 ln 55-60, col 4 ln 9-12), the method including (e.g., Figs 4 & 6, col 11 ln 21-24):

epitaxially depositing (col 10 ln 27-34, col 11 ln 23-25) semiconductor layers (112, 114, 116) that define a light emitting electrical junction on a principle surface of an epitaxy substrate (140);

forming (Fig 6D) a light-emitting device mesa (110 in Fig 5D) from the epitaxially deposited semiconductor layers;

forming a first electrode (118, col 11 ln 38) on a portion of the device mesa distal from the epitaxy substrate, the first electrode electrically contacting the device mesa;

disposing a second electrode (120) on the principle surface of the substrate;

flip-chip bonding (Fig 4) first and second electrodes to bonding pads (134, 138);

removing the epitaxy substrate (col 11 ln 27); and

subsequent to the removing of the epitaxy substrate, depositing (col 11 ln 29) an electrically conductive, light-transmissive (transparent semiconductor: col 4 ln 64-65) window layer (117) over the device mesa and the second electrode, the window layer forming an electrical connection between the device mesa and the second electrode (col 8 ln 12-23).

Re claim 23, Camras discloses etching the epitaxy substrate (140) using one of wet chemical etching and plasma etching (col 11 ln 11-15).

Re claim 26, Camras discloses a method of manufacturing a light emitting diode (col 3 ln 55-60, col 4 ln 9-12), the method including (e.g., Figs 4 & 6, col 11 ln 21-24):

depositing a plurality of semiconductor layers (112, 114, 116) including group III-phosphide layers (col 4 ln 32-33) on a GaAs substrate (140, col 10 ln 39-40);

removing at least some of the deposited semiconductor layers from a selected trench region of the deposition substrate to define a light-emissive mesa (Fig 6D);

forming an electrode (118, col 11 ln 38) on the mesa (110 in Fig 5D);

flip-chip bonding (Fig 4, col 9 ln 30-32) the mesa to a first electrical bonding pad (134) of a thermally conductive (to any extent, as per MPEP § 2111) support (130);

removing the GaAs substrate (col 11 ln 27); and

subsequent to the removing of the GaAs substrate, depositing (col 11 ln 29) a light-transmissive, electrically conductive (transparent semiconductor: col 4 ln 64-65) window layer (117) on a surface of the mesa opposite the electrode.

Re claim 27, Camras discloses the deposited light-transmissive, electrically conductive window layer extends laterally to electrically contact a second electrical bonding pad (138) of the thermally conductive support to define an electrical path between the mesa and the second electrical bonding pad (col 8 ln 12-23).

Re claim 28, Camras discloses non-epitaxially depositing (encompassed by "conventional deposition techniques", col 10 ln 60-62) at least one window layer.

Re claim 29, Camras discloses depositing at least one GaP or AlGaAs window layer (col 4 ln 67, col 5 ln 1) by liquid phase epitaxy (LPE: col 10 ln 60-62).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Camras as applied respectively to claims 2 and 7 above, and further in view of Shieh (US 5,780,321).

Re claims 3 & 8, Camras differs from the claimed invention only in not expressly disclosing an insulating material between the second bonding pad and the mesa.

Shieh discloses (e.g., Fig 2) prior to removal of the substrate (12, Fig 4-Fig 5), depositing an insulating layer (clear portions on sides of mesa must insulate) at least on sidewalls of the mesa.

Camras discloses deposition of the window layer and bonding to the bonding pads after removal of the substrate (col 11 ln 27-29).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Shieh, the method of Camras include prior to the depositing of a window layer, depositing an insulating material on at least sidewalls of the mesa and between the second electrical bonding pad and the mesa, the window layer extending laterally over the insulating material; at least to prevent possible shorts.

Response to Arguments

Applicant's arguments filed 04/19/2007 regarding Shieh lacking an additional deposition step after a substrate removal step have been fully considered and are persuasive. Therefore, the rejections based on Shieh have been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Camras.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kish (US 5,376,580) teaches the advantages of epitaxial growth on one substrate, then removal and replacement thereof with a window layer (e.g., abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571- 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system, see http://pair-direct.uspto.gov. For questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew O. Arena
23 July 2007

Sara Crane
Primary Examiner